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Clean Version of Pending Claims

DIRECT BUILD-UP LAYER ON AN ENCAPSULATED DIE PACKAGE
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1. A microelectronic package, comprising:
a microelectronic die having an active surface and at least one side;
encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;
a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and
at least one conductive trace disposed on said first dielectric material layer and in electrical contact with said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

2. The microelectronic package of claim 1, further including at least one additional dielectric material layer disposed over said at least one conductive trace and said first dielectric material layer.

3. The microelectronic package of claim 2, wherein at least a portion of said at least one conductive trace extends through and resides on said at least one additional dielectric material layer.

4. The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

24. The microelectronic package of claim 4, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

25. The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die.

26. (Amended) A microelectronic package, comprising:

a microelectronic die having an active surface, a back surface, and at least one side; and

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface.

27. The microelectronic package of claim 26, further including at least one conductive trace disposed on said first dielectric material layer and in electrical contact with said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

28. The microelectronic package of claim 26, further including at least one additional dielectric material layer disposed over said at least one conductive trace and said first dielectric material layer.

29. The microelectronic package of claim 28, wherein at least a portion of said at least one conductive trace extends through and resides on said at least one additional dielectric material layer.

30. The microelectronic package of claim 26, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

31. A microelectronic package, comprising:
a plurality of microelectronic dice each having an active surface and at least one side; and encapsulation material adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one surface substantially planar to said plurality of microelectronic dice active surfaces.

32. The microelectronic package of claim 31, further including at least one conductive trace disposed on said first dielectric material layer and in electrical contact with said microelectronic die active surface, wherein said at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

33. The microelectronic package of claim 32, further including at least one additional dielectric material layer disposed over said at least one conductive trace and said first dielectric material layer.

34. The microelectronic package of claim 33, wherein at least a portion of said at least one conductive trace extends through and resides on said at least one additional dielectric material layer.

35. The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal

contact with said microelectronic die back surface.

36. The microelectronic package of claim 35, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

37. The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die.